What is Claimed is:

1. A semiconductor integrated circuit device comprising:

a semiconductor substrate having a principal side;

a well region of at least a first-conductivity type;

a first transistor of a MIS depletion type having a first source region and a first drain region of a second-conductivity-type formed in the well region, a first channel region interposed between the first source and drain regions, a gate insulating film formed over the first channel region, and a first gate electrode formed on the first channel region over the gate insulating film, the first channel region having an impurity concentration that permits current to flow when a gate-source voltage is zero; and

a second transistor having a second channel region having the same impurity concentration as the first channel region formed in the well region, a second source region and a drain region of a second-conductivity-type respectively formed at both sides of the second channel region, and a second gate electrode formed on the second channel region over the gate insulating film,

wherein the second transistor forms part of a masked ROM.

2. A semiconductor integrated circuit device according to claim 1, further including a first LDD region of a second-conductivity-type having a lower impurity concentration than the first source region or the first drain region formed between the first channel region and the first source region and between the first channel and the first drain region, and a second LDD region of a second-conductivity-type having a lower impurity concentration than the second source region or the second drain region formed between the second channel region and the second source region and between the second channel and the second drain region.

3. A semiconductor integrated circuit device according to claim 1, further including a punch-through stopper region of a first-conductivity-type formed between the first source region and the first drain region and between the second source region and the second drain region.

4. A semiconductor integrated circuit device according to claim 2, further including a punch-through stopper region of a first-conductivity-type formed between the first source region and the first drain region and between the second source region and the second drain region.

5. A semiconductor integrated circuit device according to claim 2, further including an enhancement type NMOS transistor formed over the well region, which has a P type well region formed over the principal side of the semiconductor substrate, a third source region of an N type and a third drain region an N type formed in the P type well region, and a third channel region interposed between the third source and drain regions, a third LDD region of an N type having a lower impurity concentration than the third source region or the third drain region formed between the third channel region and the third source region and between the third channel region and the third drain region, a third gate electrode formed on the third channel region over the gate insulating film, and a P type punch-through stopper region formed between the third source region and the third drain region; and

an enhancement type PMOS transistor formed over the well region, which has an N type well region is formed at the principal side of the semiconductor substrate, a fourth source region of a P type and a fourth drain region of a P type formed in the N type well region, a fourth channel region interposed between the fourth source and drain regions, and a fourth LDD region of a P type having a lower impurity concentration than the fourth source region or the fourth drain region formed between the fourth channel region and the fourth source region and between the fourth channel region and the fourth drain region, a fourth gate electrode formed on the fourth channel region over the gate insulating film, and an N type punch-through stopper region formed between the fourth source region and the fourth drain region.

6. A semiconductor integrated circuit device according to claim 5, further including a first-conductivity-type punch-through stopper region provided between the first source region and the first drain region.

7. A semiconductor integrated circuit device according to claim 6, further including a first-conductivity-type punch-through stopper region provided between the second source region and the second drain region.

8. A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a first transistor of a MIS depletion type and a second transistor forming part of a masked ROM on a single semiconductor substrate by:

forming a well region of a first-conductivity-type in a first region where the first transistor is to be formed and a second region where the second transistor is to be formed;

selectively oxidizing the regions where the first and second transistors are to be formed;

implanting impurity ions of a first-conductivity-type in the regions where the first and second transistors are to be formed;

implanting impurity ions of a second-conductivity-type in the regions where the first and second transistors are to be formed to permit current to flow when a gate-source voltage of the first transistor is zero; and

forming a gate insulating film, a gate electrode, and source and drain regions of a second-conductivity-type in each of the first and second transistors.